Preliminary(1)

NEC

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NP50C1MF01 Data Sheet

127 cm (50 type), Wide screen (1365 x 768 Pixels), Digital Module
Digital RGB signal, 8bits signal each

DESCRIPTION

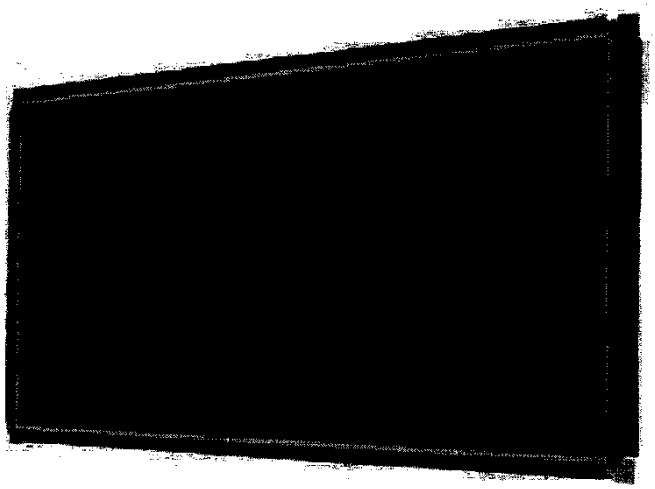
The NP50C1MF01 is a 50-inch wide color plasma display module with a resolution of 1365(H)x768(V) pixels. The display offers vibrant colors we reproduced in a thin and low profile package. This device uses AC plasma technology by NEC and includes an 8-bit of digital video signal interface for each RGB color.

FEATURES

- ☐ Applied Capsulated Color Filter (CCF) technology, developed at NEC, which offers a high quality image match for CRT display. To offer remarkably pure colors, the color plasma display panel uses extremely clear, thin capsulated color filters to cut unnecessary light as the plasma discharges.
- ☐ Peak luminance of 450cd/m^2 (typical value) is achieved through a new deriving method, which offers extremely vivid image with good contrast.
- ☐ Applied Peak Luminance Enhancement (PLE) function that enables the display to operate with the ideal contrast. The PLE function makes it possible to adjust the average luminance level of the PDP display automatically in accordance with the average luminance level of an input video signal.

APPLICATIONS

- ☐ Wide Screen TV (aspect ratio 16:9)
- ☐ Public Information Display
- ☐ Video Conference Systems
- ☐ Retail
- ☐ Education and Training Systems



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STRUCTURE AND PRINCIPLE OPERATION OF PLASMA DISPLAY

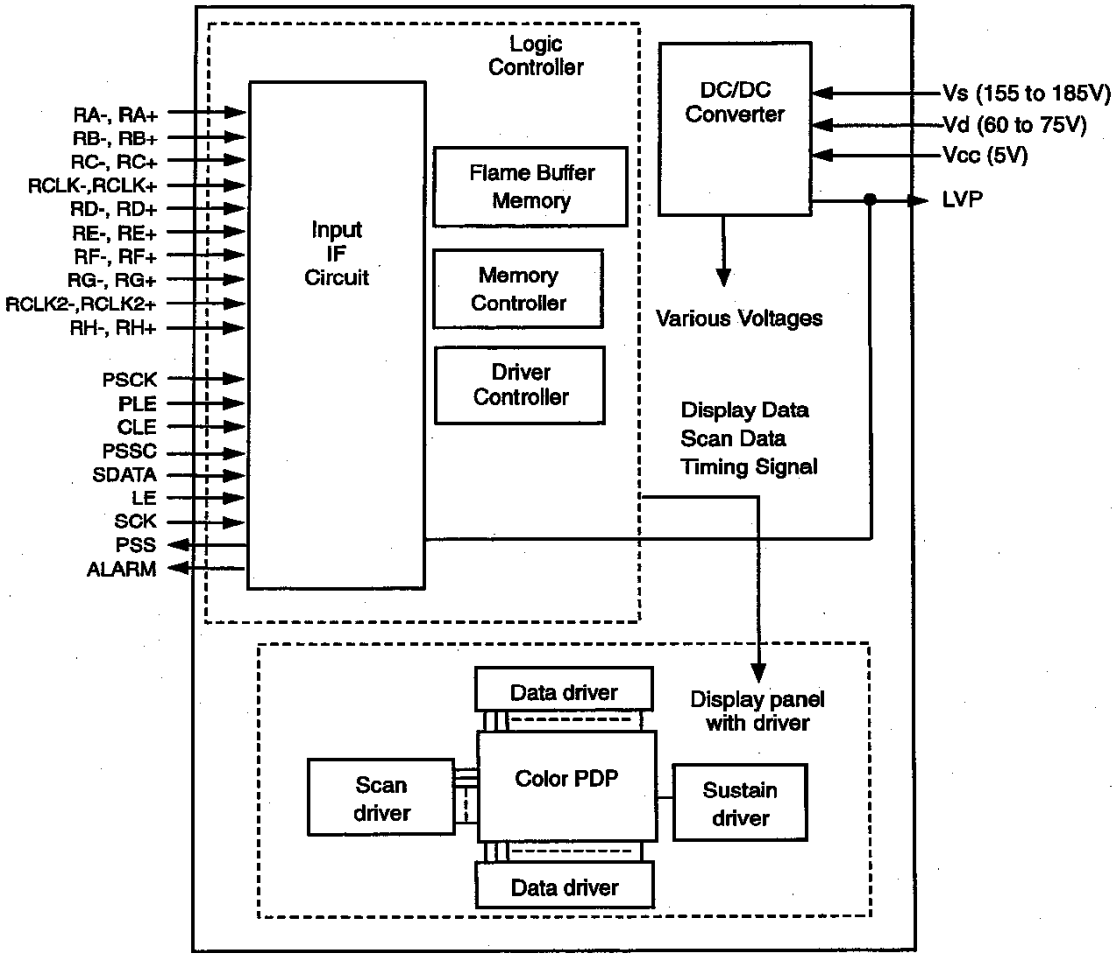
In a Plasma Display Panel, Row and Column electrodes are placed between two glass substrates. A rare gas is then filled between each substrate. When a high voltage is applied to these electrodes, the gas is activated resulting in the radiation of ultraviolet light, similar to the operation in fluorescent lamps. These ultraviolet rays then activate phosphor that has been coated on the inside of the glass substrate, and visible light is emitted from the panel.

ELECTRICAL INTERFACE OF PLASMA DISPLAY

NP50C1MF01 requires 8 bits of digital video signals for each RGB color. For the signal inputs, serial interface (LVDS video signal) is prepared in the module. In addition to the video signals, synchronous signals, mode control signals and 3 different DC voltages are required to operate the display.

This plasma display module has a "PLE" (Peak Luminance Enhancement) function that adjusts the luminance and contrast to the suitable value in accordance with the input video signal level variance, so that images can be displayed with the ideal luminance and contrast.

BASIC CONFIGURATION



GENERAL SPECIFICATION

Display area	1106(H) x 622(V) mm
Outline dimensions	1191(W) x 714(H) x 50(D) mm
Weight	24 kg
Aspect ratio	16:9
Number of pixels	1365(H) x 768(V) (1pixel = 3 RGB cells)
Pixel pitch	0.81 (H) x 0.81(V) mm
Color arrangement	RGB vertical stripes
Number of gradations	256 steps for each RGB
Peak luminance	450cd/m^2 typical (Video signal*, 0.5% white window, PLE** mode set to the maximum)

* Signal of EUTV mode : fv = 59.94 Hz and fh = 31.47 kHz
** See PLE (Peak Luminance Enhancement) description.

OPERATION ENVIRONMENTAL CONDITIONS

Temperature	0 to 60 °C (with forced-air cooling)
Humidity	20 to 80% R.H. (without condensation)
Atmospheric pressure	800 to 1100 hPa

STORAGE ENVIRONMENTAL CONDITIONS

Temperature	-20 to 60 °C
Humidity	10 to 90% R.H. (without condensation)
Atmospheric pressure	700 to 1100 hPa

MECHANICAL TEST CONDITIONS

Vibration (operating)	4.9m/s^2(0.5 G), 10 to 100 Hz, 3 directions, 10 minutes each
Vibration (non-operating)	4.9m/s^2(0.5 G), 10 to 100 Hz, 3 directions, 2 hours each

LIFE EXPECTANCY

More than 10,000 hours of continuous operation
(Time when the luminance decreased to half of the initial)

POWER INPUT AND OUTPUT

1) Sustain Power Supply

Table 1. Power Output

Item	Symbol	Condition and Remarks	Min.	Typ.	Max.	Unit
Absolute Maximum	----	--------	----	----	200	V
Voltage	Vs	Dependent on the characteristics of each PDP (Note1)	155	----	185	V
Voltage Stability	----	--------	----	----	±1.0	%
Average Current (Note2)	Is-a	Under normal PLE operation	0.1	----	3.0	A
Average current at inhibited PLE operation (Note 2)	Is-ple	(Reference value) (Note3)	----	----	T.B.D	A
Peak Current	Is-peak	--------	----	----	21	A
Voltage Regulation	----	At peak current	----	----	T.B.D	V
Ripple and Noise	----	--------	----	----	T.B.D	mVp-p

Note1: Voltage should be set to a specified value, which is located on a label attached to the module.
Note2: Average of rippled current.
Note3: See PLE (Peak Luminance Enhancement) description.
Current when PLE is set to maximum luminance level with full white image, or when PLE has a delayed response and image is changed from full black to full white.

2) Data Power Supply

Table 2. Data Power Supply

Item	Symbol	Condition and Remarks	Min.	Typ.	Max.	Unit
Absolute Maximum	----	----	----	----	90	V
Voltage	Vd	Dependent on the characteristics of each PDP	60	----	75	V
Voltage Stability	----	----	----	----	±1.5	%
Average Current (Note2)	Id-a	Varied correspondence to the Image	0.005	----	1.5	A
Peak Current	Id-peak	----	----	----	T.B.D.	A
Ripple and Noise	----	----	----	----	T.B.D	mVp-p

Note1: Voltage should be set to a specified value, which is located on a label attached to the module.
Note2: Average of rippled current.

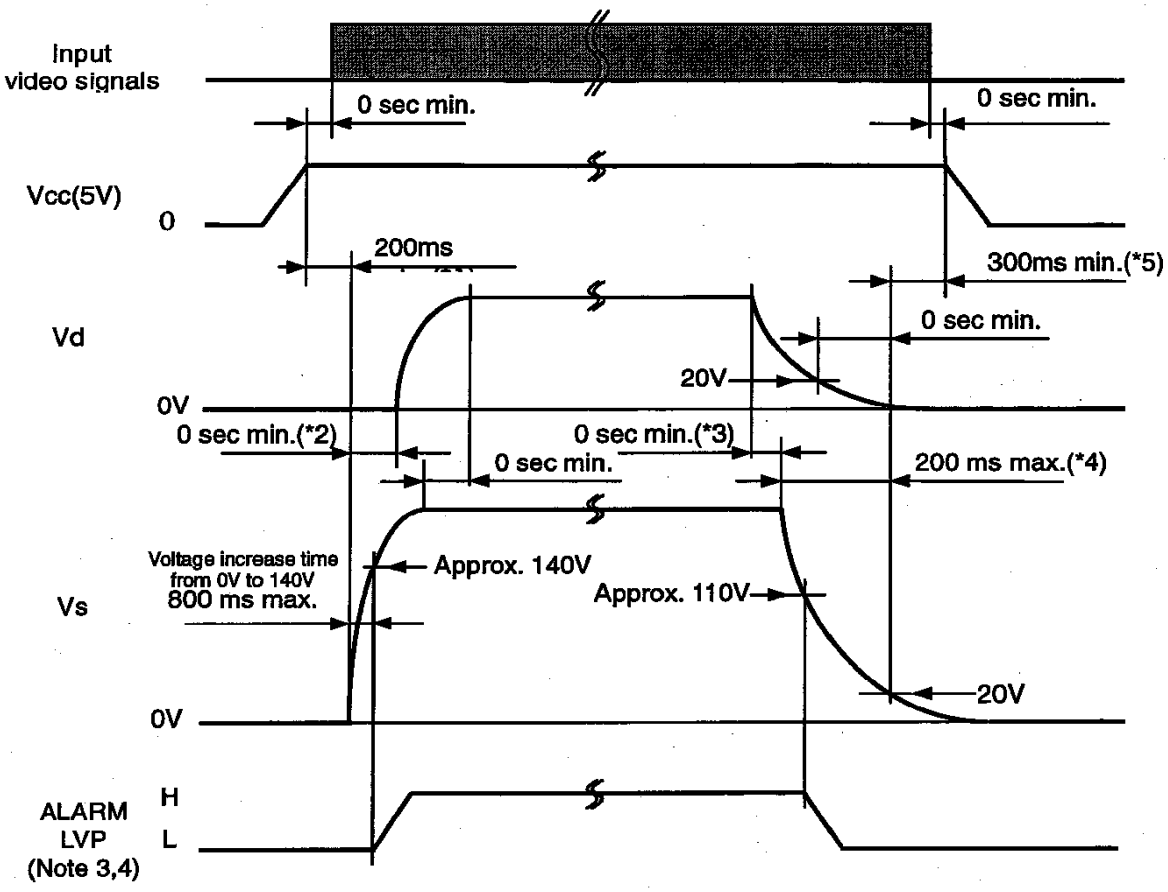
3) Logic Power Supply

Table 3. Logic Power Supply

Item	Symbol	Condition and Remarks	Min.	Typ.	Max.	Unit
Absolute Maximum	----	--------	4.5	----	6.0	V
Voltage Range	Vcc	--------	4.75	5.0	5.25	V
Current (Note1)	Icc	--------	----	----	6.0	A
Peak Current	Icc-peak	--------	----	----	T.B.D.	A
Ripple	----	--------	----	----	30	mVp-p
Noise	----	--------	----	----	300	mVp-p

Note1: Average of rippled current.
This module provides an automatic operation-stop function for internal malfunctions. When the module stops the operation, logic current may reduce to almost zero (0). Even if logic current becomes zero, applied voltage should be kept to less than 6.0 volts.

SUPPLY VOLTAGE AND SIGNAL SEQUENCE



Note 1: Power ON/OFF sequence is as follows (refer to the above sequence diagram):

Power ON sequence:
Vcc ON → 200ms min.(*1) → Vs ON → 0sec min.(*2) → Vd ON
Power OFF sequence:
Vd OFF → 0sec min. (*3) → Vs OFF → 200ms max.(*4) → 300ms min.(*5) → VccOFF

(Caution)
If power sequence does not meet to above sequence diagram, PDP drivers may have a permanent damage.
In order to decrease Vs and Vd voltages quickly to satisfy above sequence diagram, forced discharge circuits are essential in the power supply.

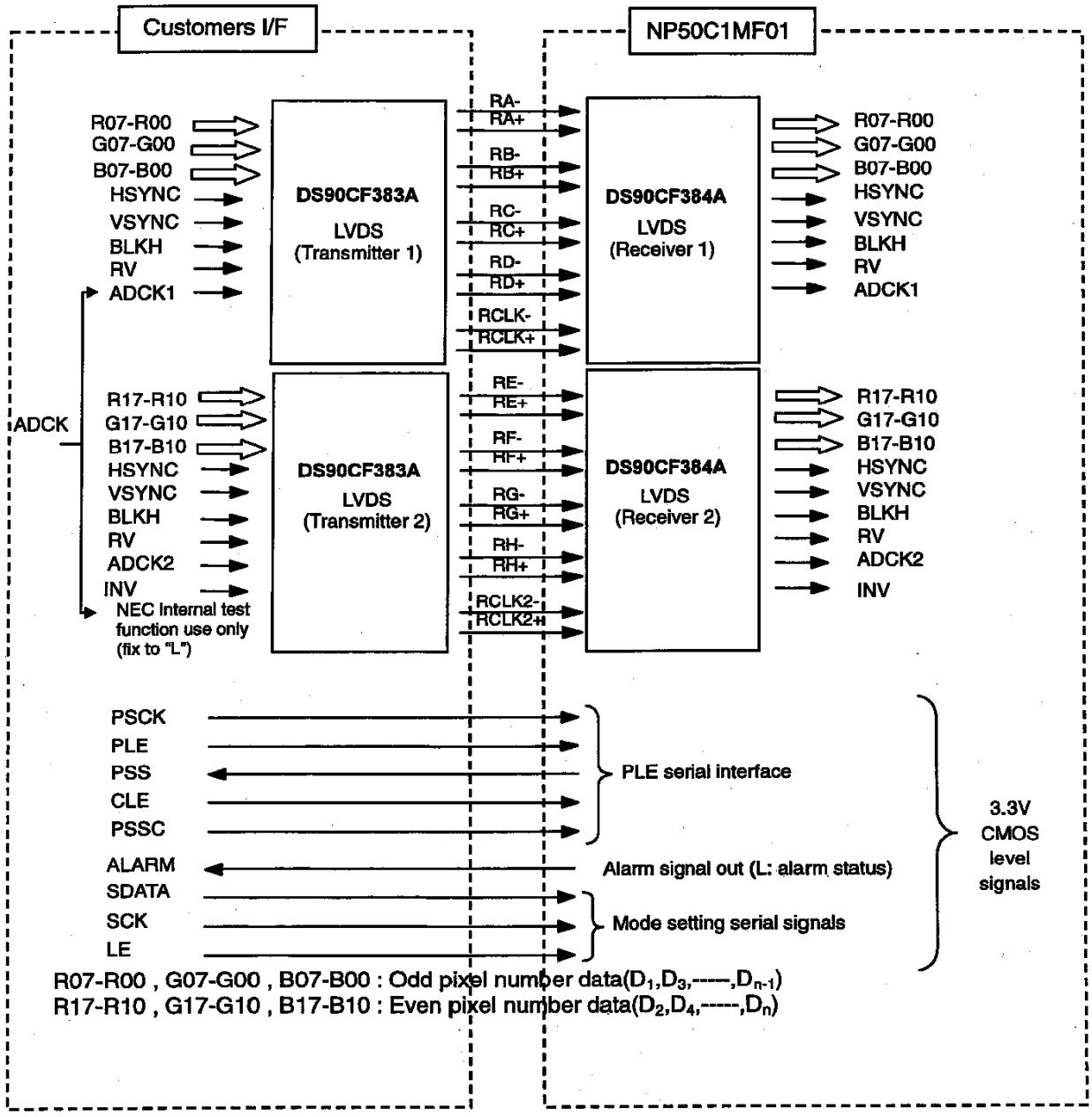
Note 2: The power source for the Input signal circuit and Vcc can be switched on and off at the same time.

Note 3: LVP is the power supply shutdown output signal when the panel is broken and/or failure of internal power source in the PDP module.

Note 4: When the ALARM and LVP signals are "L" High voltage should be shut down. However, when Vcc is applied at first, ALARM and LVP signals are kept "L" until Vs is applied. In order to enable "high voltage power supply" operation, the initial ALARM and LVP signals' status "L" should be disregarded.

INTERFACE SIGNAL

SERIAL INTERFACE CONFIGURATION



ELECTRICAL CHARACTERISTICS

1) Interface Signals; Absolute Ratings

Common conditions: Ta=25ºC, Vcc=5V

Table 4. Absolute Ratings

Item			Parameter	Symbol	Ratings	Unit
Input Signals	LVDS	RA-, RA+, RB-, RB+, RC-, RC+, RD-, RD+, RCLK-, RCLK+ RE-, RE+, RF-, RF+, RG-, RG+, RH-, RH+, RCLK2-, RCLK2+	Input Voltage	Vi	-0.3 to 3.6	V
			Input current	Ii		mA
	3.3V CMOS	SDATA, SCK, LE	Input Voltage	Vi	-0.5 to 4.6	V
			Input current	Ii	±15	mA
		PSCK, PLE, CLE, PSSC	Input Voltage	Vi	-0.5 to 4.6	V
			Input current	Ii	±15	mA
Output Signals	3.3V CMOS	PSS	Output Voltage	Vo	-0.5 to 3.5	V
			Output current	Io	±20	mA
		ALARM	Output Voltage	Vo	-0.5 to 3.5	V
			Output current	Io	±20	mA

2) Interface Signals; Electrical Characteristics

Common conditions: Ta=25ºC, Vcc=5V

Table 5. Electrical Characteristics

Signal	Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
LVDS	High Level Input Voltage	V_{TH}	V_{CM}=1.2V	---	---	100	mV
	Low Level Input Voltage	V_{TL}	V_{CM}=1.2V	-100	---	---	mV
	Input Current	I_{IN}	V_{IN}=+2.4/GND	---	---	±10	µA
3.3V CMOS	High Level Input Voltage	V_{IH}	-----	2.0	---	---	V
	Low Level Input Voltage	V_{IL}	-----	---	---	0.8	V
	Input Current	I_i	V_i=V_{CC} or GND	---	---	±5.0	µA
	High Level Output Voltage	V_{OH}	I_o=1mA	2.4	---	---	V
	Low Level Output Voltage	V_{OL}	I_o=1mA	---	---	0.4	V

INPUT SIGNAL FUNCTION of LVDS TRANSMITTER (DS90CF383A)

Table 6. Interface Signal Function

Symbol	Function	(Remarks)
R07 to R00	8 bits red video signal (Note 1)	(R07:MSB*, R00: LSB**)
R17 to R10	8 bits red video signal (Note 1)	(R17:MSB*, R10: LSB**)
G07 to G00	8 bits green video signal (Note 1)	(G07:MSB*, G00:LSB**)
G17 to G10	8 bits green video signal (Note 1)	(G17:MSB*, G10:LSB**)
B07 to B00	8 bits blue video signal (Note 1)	(B07:MSB*, B00:LSB**)
B17 to B10	8 bits blue video signal (Note 1)	(B17:MSB*, B10:LSB**)
ADCK1,2	Clock for video signal	(latch the video signal at falling edge)
HSYNC	Horizontal synchronous signal tw=4TADCK min.	(negative pulse)
VSYNC	Vertical synchronous signal tw=200ns min.	(negative pulse)
BLKH	Video blanking and/or muting (Note 2)	("H" in blanking, muting)
RV	Reverse the RGB video data polarity	(Set to "L" level for normal use)
INV	NEC internal test function use only	(Fix to "L" level)

* MSB: Most Significant Bit
** LSB: Least Significant Bit
Note 1: The RGB video signal should be compensated with Inverseγcircuit before input to the color plasma display module.
Note 2: While BLKH input is "H" level, all display area image turns to black color display.

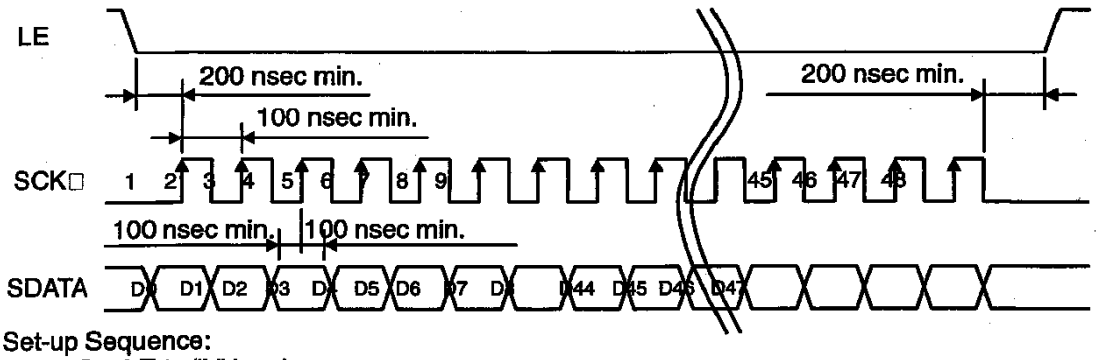
INPUT SIGNAL FUNCTION of PDP MODULE (NP50C1MF01)

Table 7. Interface Signal Function

Symbol	I/O	Function	(Remarks)
RA-	I	Video signal input A-	LVDS signal 1
RA+	I	Video signal input A+	LVDS signal 1
RB-	I	Video signal input B-	LVDS signal 1
RB+	I	Video signal input B+	LVDS signal 1
RC-	I	Video signal input C-	LVDS signal 1
RC+	I	Video signal input C+	LVDS signal 1
RD-	I	Video signal input D-	LVDS signal 1
RD+	I	Video signal input D+	LVDS signal 1
RCLK-	I	Clock signal clock-	LVDS signal 1
RCLK+	I	Clock signal clock+	LVDS signal 1
RE-	I	Video signal input E-	LVDS signal 2
RE+	I	Video signal input E+	LVDS signal 2
RF-	I	Video signal input F-	LVDS signal 2
RF+	I	Video signal input F+	LVDS signal 2
RG-	I	Video signal input G-	LVDS signal 2
RG+	I	Video signal input G+	LVDS signal 2
RH-	I	Video signal input H-	LVDS signal 2
RH+	I	Video signal input H+	LVDS signal 2
RCLK2-	I	Clock signal clock-	LVDS signal 2
RCLK2+	I	Clock signal clock+	LVDS signal 2
SDATA	I	Mode setting serial data	(48-bit)
SCK	I	Clock signal for SDATA	
LE	I	SDATA write enable	("L" in SDATA write)
PSCK	I	Clock signal for PSS, PSSC serial data	(latch in positive edge)
PLE	I	PSS data read enable	("L" in PSS data read)
PSS	O	PLE average luminance signal	(9-bit)
CLE	I	PSSC data write enable	("L" in data write)
PSSC	I	PLE luminance control data	(8-bit)
ALARM	O	Alarm signal for panel broken and failure of internal power-source. (Note 1)	("L" in alarmed status)

Note 1: When ALARM output turns to "L" level, high voltage power input (Sustain power supply: Vs, and Data power supply: Vd) should be switched off immediately. When glass panel is broken, high voltage may occur at the electrode section and cause electric shock. Failure of internal power-source causes over-power status and gives damage to the display panel and driver-circuits.

SET-UP OF CONTROL MODE SIGNALS AND DISPLAY POSITION



Set-up Sequence:

1. Set LE to "L" level.
2. Enter the 48 bits of SDATA into the module synchronizing to the serial clock signal (SCK)
3. Set LE to "H" level.

Note 1: SCK clock rate: 1MHz max.

Note 2: Serial input data should be refreshed at least in every 5 or 6 seconds or less.

Note 3: Serial input data (SDATA) is latched into the module at the falling edge of the VSYNC signal after "LE" signal is returned back to "H" level. When VSYNC is overlapped with the "LE" signal's "L" period, the serial data is latched with the next VSYNC timing.

Note 4: When only 48 SCK clocks are entered while LE is "L" level period, SDATA become enabled, If SCK clocks number is not 48, SDATA is not refreshed.

Note 5: When powers are supplied to the module, serial data in the module has vague status. Therefore serial data should be refreshed after powered on.

MODE SETTING SIGNALS

Table8. Contents of SDATA (Mode setting serial input data)

SDATA	Signal name	Function	Remarks
D0	Spate bit	Fix to "L" level	
D1	CODE 2	Subfield length selection bits	PC(56 to 75Hz) Video(50Hz) Video(56-64Hz) CODE2 L L L CODE1 L L H CODE0 L H L
D2	CODE 1		
D3	CODE 0		
D4	PRI M1	NEC Internal test use only	Fix to "H"
D5	PRI M0	NEC internal test use only	Fix to "H"
D6	SAFEL	NEC internal test use only	Fix to "L"
D7	LIFEH	Switch for PLE luminance level	L: PLE normal operation H: Fix PLE to low luminance level for longer life operation
D8	Spare bit	Fix to "L" level	
D9	SELFPLEH	Switch for "Internal PLE" and "External PLE"	H: Internal PLE control L: External PLE control
D10	TSELB	Switch for ADCK data latch timing	Fix to "H" (H: Falling edge L: Rising edge)
D11	FV 2	Vertical frequency selection bits	(Hz) 50 56-64□ 66□ 67-71 72-75 FV2 L L L L H FV1 L L H H L FV0 L H L H L
D12	FV 1		
D13	FV 0		
D14	DISPLINE 2	Display line number	line 400 480 600 624 720 768 640 DL2 L L L L H H H DL1 L L H H L L H DL0 L H L H L H L
D15	DISPLINE 1		
D16	DISPLINE 0		
D17	DISPDOT 2	Display pixel number/line	Pixels 640 800 832 853 864 1024 1280 1365 DD2 L L L L H H H H DD1 L L H H L L H H DD0 L H L H L H L H
D18	DISPDOT 1		
D19	DISPDOT 0		
D20	VDELAY 256	Display start vertical position Refer to the "Dv" in the table 9	Set the display start line numbers after the falling edge of the VSYNC. Range of setting line numbers: 0 to 511 This number should not exceed the total line numbers in one frame period (1V).
D21	VDELAY 128		
D22	VDELAY 64		
D23	VDELAY 32		
D24	VDELAY 16		
D25	VDELAY 8		
D26	VDELAY 4		
D27	VDELAY 2		
D28	VDELAY 1		
D29	HDELAY 512	Display start horizontal position Refer to the "Dh" in the table 9	Set the display start pixel numbers after the falling edge of the HSYNC. Range of setting line numbers: 0 to 1023 This number should not exceed the total line numbers in one line period (1H).
D30	HDELAY 256		
D31	HDELAY 128		
D32	HDELAY 64		
D33	HDELAY 32		
D34	HDELAY 16		
D35	HDELAY 8		
D36	HDELAY 4		
D37	HDELAY 2		
D38	HDELAY 1		
D39	HPOS 3	Setting of horizontal display position in normal mode (640-pixel/line display).Display position is adjustable by 2 pixel steps.	Position Left -------- Center -------- Right POS3 L L L □□□ H □□□ H H H POS2 L L L □□□ L □□□ H H H POS1 L L H □□□ L □□□ L H H POS0 L H L □□□ L □□□ H L H
D40	HPOS 2		
D41	HPOS 1		
D42	HPOS 0		
D43	MASKLEVEL 3	Gray level in black area (Possible to set 0-20% of white level)	Level(%) Dark ---------- Light ML2 L L L L L L L H H H H H H H H ML1 L L L L H H H H L L L L H H H H ML0 L L H H L L H H L L H H L L H H MLL L H L H L H L H L H L H L H L H
D44	MASKLEVEL 2		
D45	MASKLEVEL 1		
D46	MASKLEVEL 0		
D47	Spare bit	Fix to "L" level	

EXAMPLE OF VIDEO SIGNAL INPUT AND SIGNAL TIMING

Table 9. Relation Between Input Video Signal and Module RGB Signal Input

		Video signal standard format (reference)						Module input data timing mode signals											
											Mode signal				Nominal data read start timing of the sync. signal		Standard video start timing after the synchronous signal	
No.		Signal name		Display resolution (dot line)	Vertical Synchronous frequency	Total numbers of dots and lines	Horizontal Synchronous frequency	Display resolution (dot line) (n.m)	Horizontal Synchronous frequency f_H(kHz)	Recommended clock frequency (MHz) and number of clocks for 1H (Note1)	VIDEO	FV	DL	DD	VD std. (line)	HD std. (dot)	Dv	Dh
VIDEO MODE	1	EU1		576line	50.00	625/2 lines	15.625	1365□768	41.67	69.3/2 (832)	1	0	5	7	59	263	60	136
	2	EDTV		480line	59.94	525/2 lines	15.734	1365□768	50.35	83.8/2 (832)	1	1	5	7	53	236	54	123
	3	HDTV		1035line	60.00	2200□1125 /2	33.75	1365□768	50.63	80.03/2 (791)	1	1	5	7	59	159	60	84
	4	ATV-I		1920□1080	60.00/ 59.94	2200□1125 /2	33.75 / 33.72	1365□768	50.61	83.51/2 (825)	1	1	5	7	29	167	30	88
	5	ATV-P		1280□720	60.00 / 59.94	1650□750	45.00 / 44.96	1280□720	45.00	74.25/2 (825)	1	1	4	6	24	290	25	150
PC MODE	6	NEC		640□400	56.42	848□440	24.83	640□400	24.83	21.05/2 (424)	0	1	0	0	32	139	33	74
	7	NEC		640□400	70.09	800□449	31.47	640□400	31.47	25.17/2 (400)	0	2	0	0	35	133	36	71
	8	IBM		640□400	70.09	800□449	31.47	640□400	31.47	25.17/2 (400)	0	2	0	0	35	136	36	73
	9	VGA		640□480	59.94	800□525	31.47	640□480	31.47	25.17/2 (400)	0	1	1	0	34	134	35	72
	10	IBM		640□480	59.94	800□525	31.47	640□480	31.47	25.17/2 (400)	0	1	1	0	26	126	27	68
	11	NEC		640□480	59.94	800□525	31.47	640□480	31.47	25.17/2 (400)	0	1	1	0	38	135	39	72
	12	MAC		640□480	66.67	864□525	35.00	640□480	35.00	30.24/2 (432)	0	2	1	0	41	150	42	80
	13	VESA		640□480	72.81	832□520	37.86	640□480	37.86	31.5/2 (416)	0	3	1	0	30	158	31	84
	14	VESA		640□480	75.00	840□500	37.5	640□480	37.5	31.5/2 (420)	0	3	1	0	18	174	19	92
	15	IBM		640□480	75.00	800□525	39.38	640□480	39.38	31.5/2 (400)	0	3	1	0	33	134	34	72
	16	VESA		800□600	56.25	1024□625	35.16	800□600	35.16	36.0/2 (512)	0	1	2	1	23	190	24	100
	17	VESA		800□600	60.32	1056□628	37.88	800□600	37.88	40.0/2 (528)	0	1	2	1	26	206	27	108
	18	VESA		800□600	72.19	1040□666	48.08	800□600	48.08	50.0/2 (520)	0	3	2	1	28	174	29	92
	19	VESA		800□600	75.00	1056□625	46.88	800□600	46.88	49.5/2 (528)	0	3	2	1	23	230	24	120
	20	MAC		832□624	74.55	1152□667	49.72	832□624	49.72	57.3/2 (576)	0	3	3	2	41	278	42	144
	21	VESA		1024□768	60.00	1344□806	48.36	1024□768 1365□768	48.36 48.36	65.0/2 (672) 86.7/2 (896)	0 0	1 1	5 5	5 7	34 34	286 385	35 35	148 197
	22	EWS/L		1024□768	60.08	1344□806	48.36	1024□768 1365□768	48.36 48.36	65.0/2 (672) 86.7/2 (896)	0 0	1 1	5 5	5 7	33 33	270 363	34 34	140 186
	23	VESA		1024□768	70.07	1328□806	56.48	1024□768 1365□768	56.48 56.48	75.0/2 (664) 100.0/2 (886)	0 0	2 2	5 5	5 7	34 34	270 363	35 35	140 186
	24	□		1024□768	71.96	1376□808	58.14	1024□768 1365□768	58.14 58.14	80.0/2 (688) 106.7/2 (918)	0 0	3 3	5 5	5 7	37 37	202 273	38 38	106 141
	25	VESA		1024□768	75.03	1312□800	60.02	1024□768 1365□768	60.02 60.02	78.75/2 (656) 105.0/2 (875)	0 0	3 3	5 5	5 7	30 30	262 353	31 31	136 181
	26	MAC		1024□768	75.00	1328□803	60.24	1024□768 1365□768	60.24 60.24	80.0/2 (664) 106.7/2 (886)	0 0	3 3	5 5	5 7	32 32	262 353	33 33	136 181
	27	IBM		1024□768	75.78	1408□806	61.08	1024□768 1365□768	61.08 61.08	86.0/2 (704) 114.7/2 (936)	0 0	3 3	5 5	5 7	37 37	366 491	38 38	188 250

Note 1: Maximum data clock (ADCK) frequency is 57MHz.

Note 2: Maximum horizontal frequency in Video mode is 54 kHz

Note 3: Maximum horizontal frequency in PC mode is 65 kHz

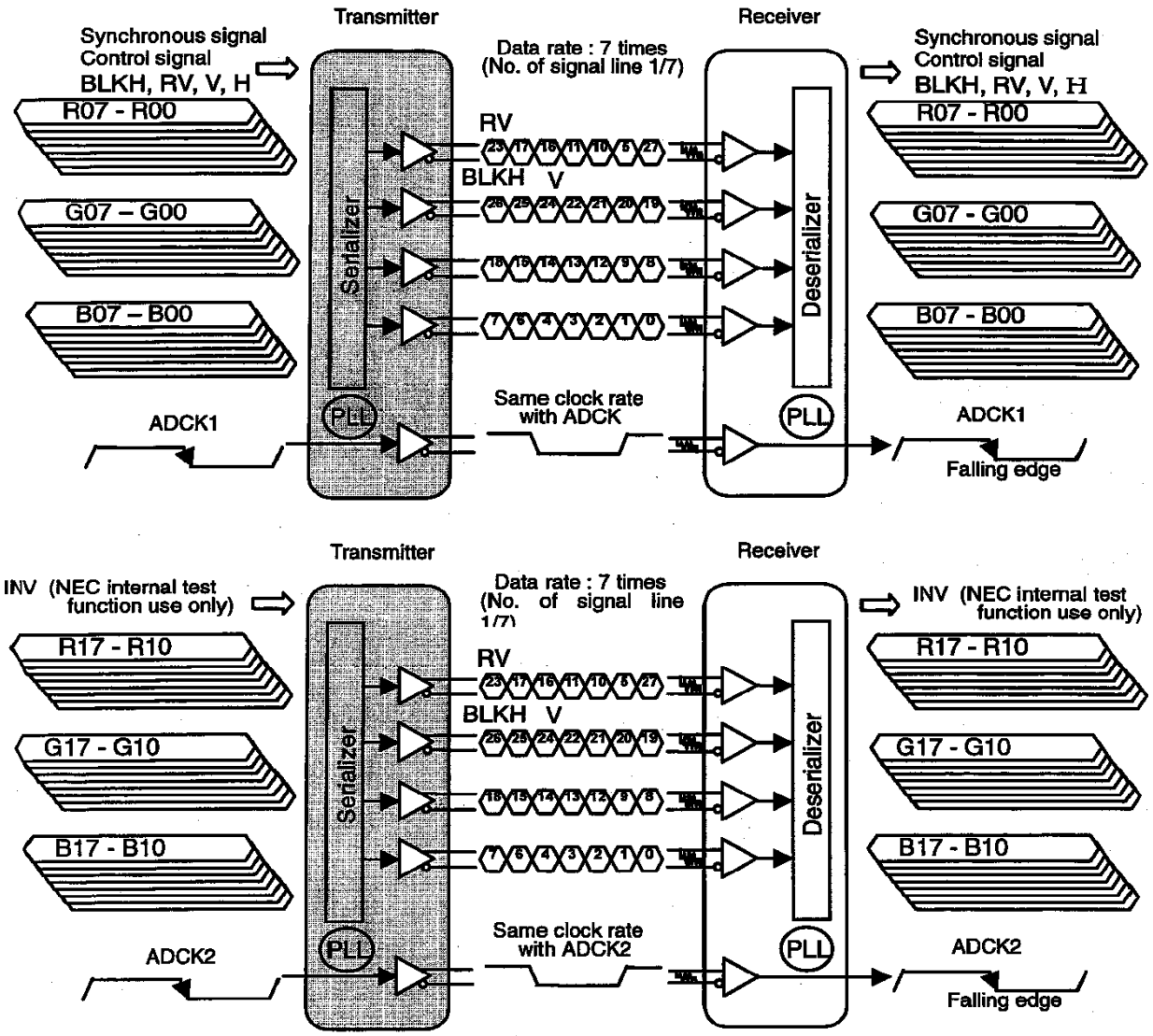
Note 4: Vertical frequency range is 50Hz to 76Hz.

Note 5: D14 to D19 (Display lines number and Display pixel number/line) of serial input data should be set correctly according to the display data. If not done correctly, PLE function is not operated correctly.

Note 6: When one horizontal signal period is divided equally with the value of above "Recommended dot clock numbers in one horizontal period", the effective display width of the video signal becomes equal with the width of the screen width. When over-scan is required, this value should be adjusted to smaller value.

Note 7: When one horizontal signal period is divided equally with the value of above "Recommended dot clock numbers in one horizontal period", Dv and Dh values in the same row gives the display image position at almost the center of the screen.

LVDS (FPDLINK) DATA TRANSFER FORMAT



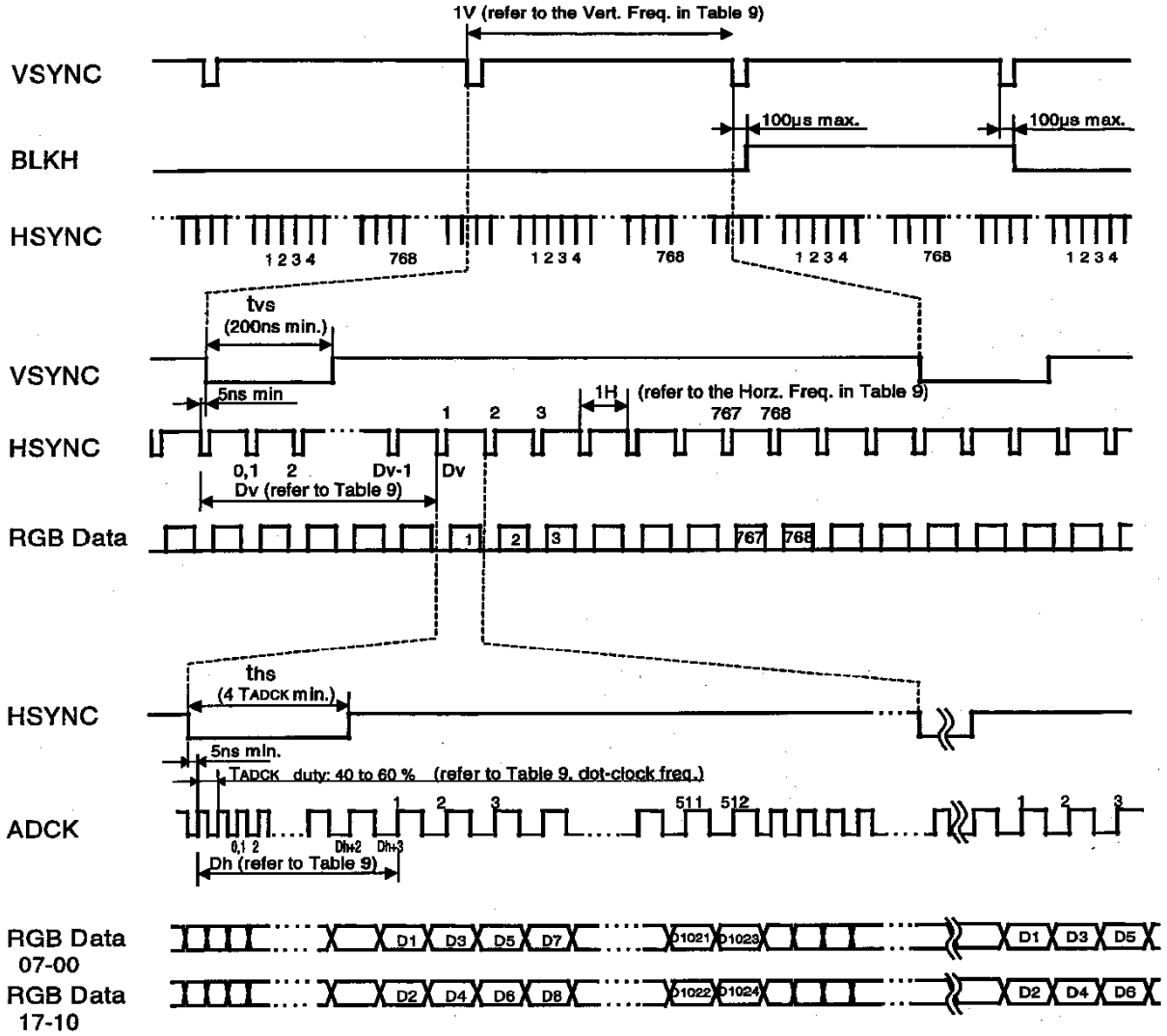
(As for detail of LVDS interface, please refer to www.national.com.)

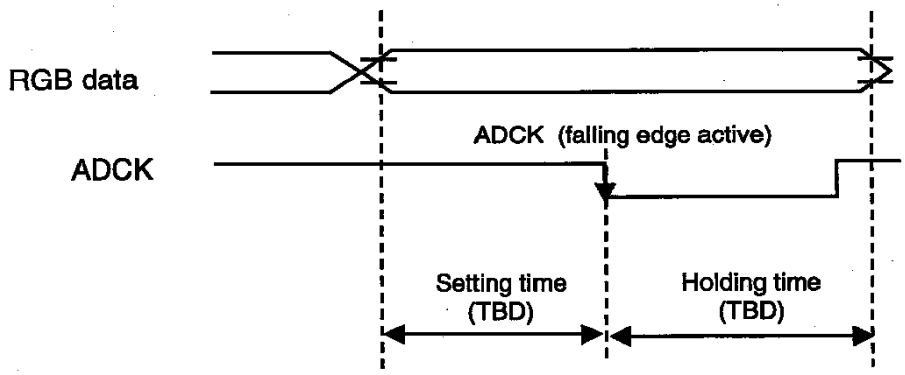
SIGNAL TIMING

Refer to the timing diagram on the following pages.

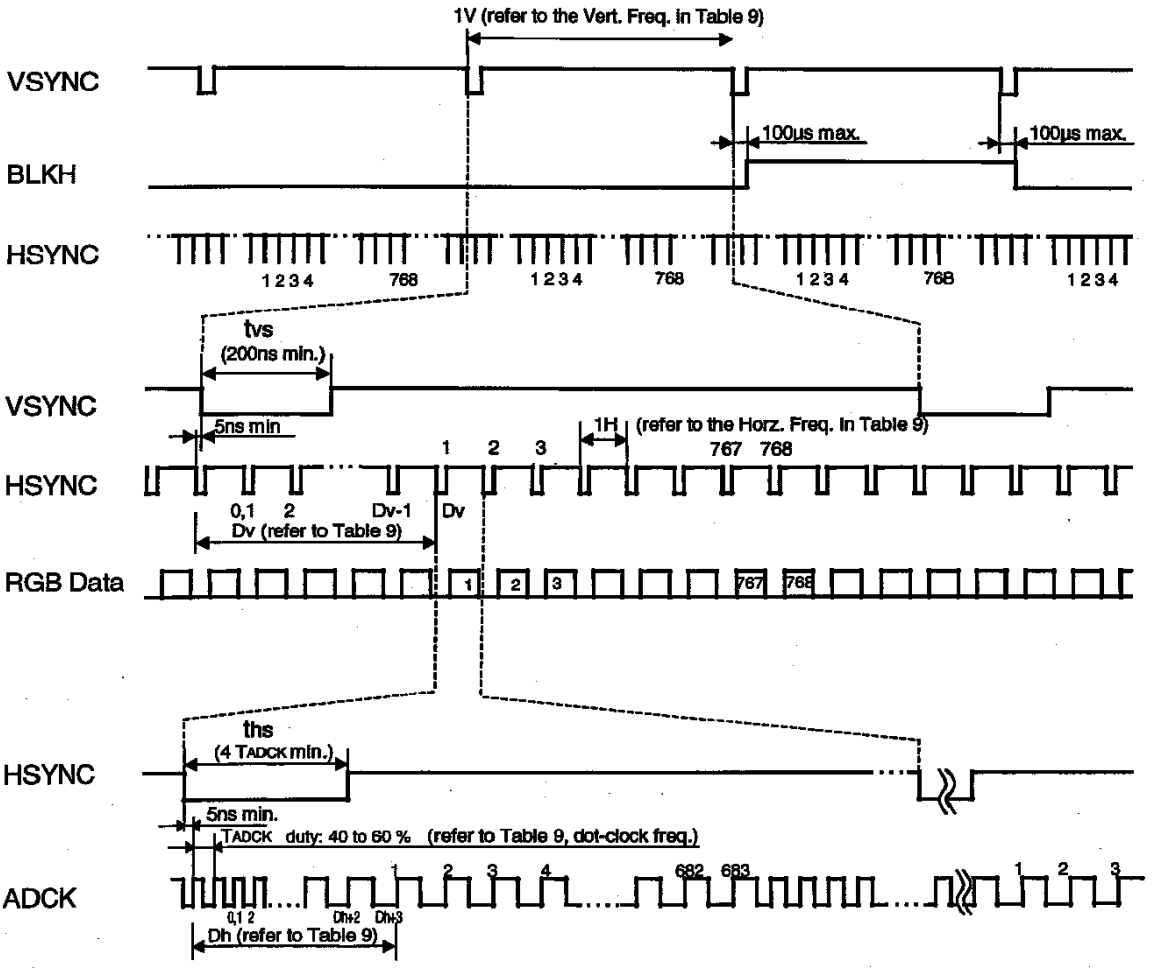
- ☐ Input video signal format is determined by Mode signal (refer to Table 9)
- ☐ "TADCK" shows 1 cycle period of ADCK.
- ☐ "tvs" shows negative pulse width of VSYNC.
- ☐ "tvh" shows negative pulse width of HSYNC.
- ☐ "1H" shows 1 cycle period of HSYNC (Horizontal Synchronous Signal).
- ☐ "1V" shows 1 cycle period of VSYNC (Vertical Synchronous Signal).
- ☐ "Dv" is a period between "leading-edge of the vertical synchronous pulses" and " valid RGB lines data read start timing "
- ☐ "Dh" is a period between "leading-edge of the horizontal synchronous pulse" and " valid RGB dots data read start timing "
- ☐ In case of normal mode (1024 dot mode) is selected, both sides are masked with gray patterns.

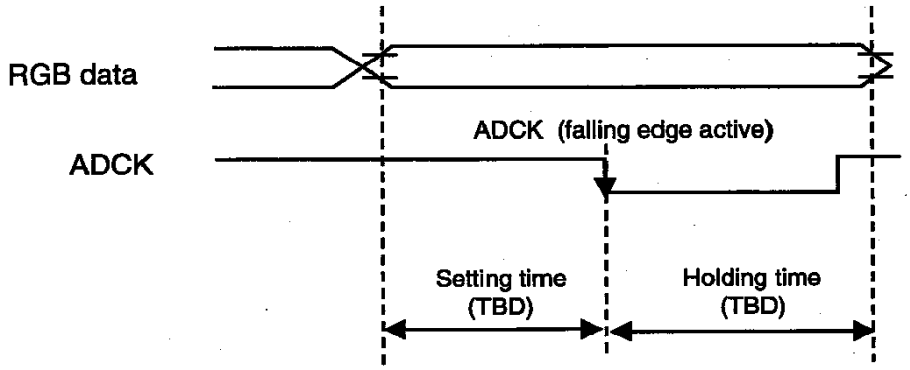
TIMING DIAGRAM (Normal Display Mode)





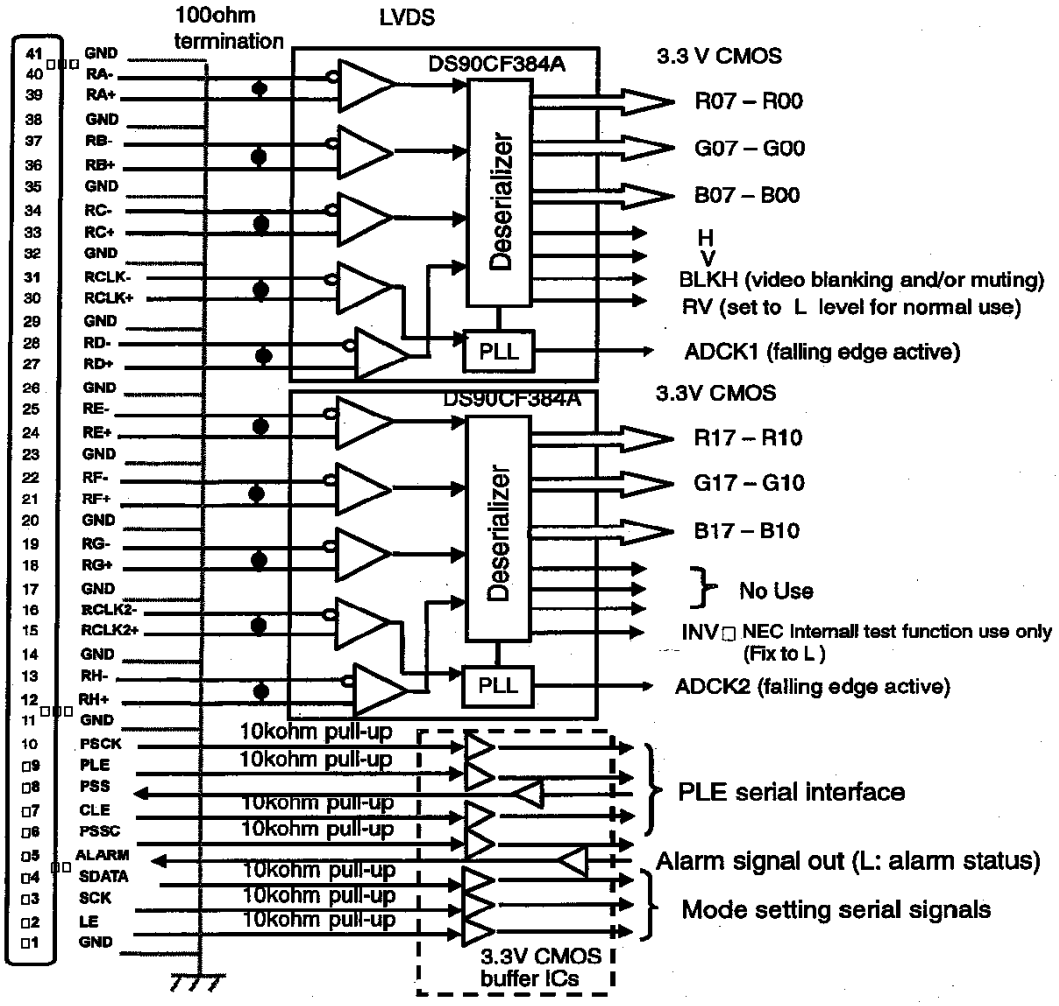
TIMING DIAGRAM (Full Display Mode)





INTERFACE CONNECTOR PIN ASSIGNMENT AND INPUT OUTPUT CIRCUITS

Following shows the interface connector pin assingnment and input output circuits in the PDP module.

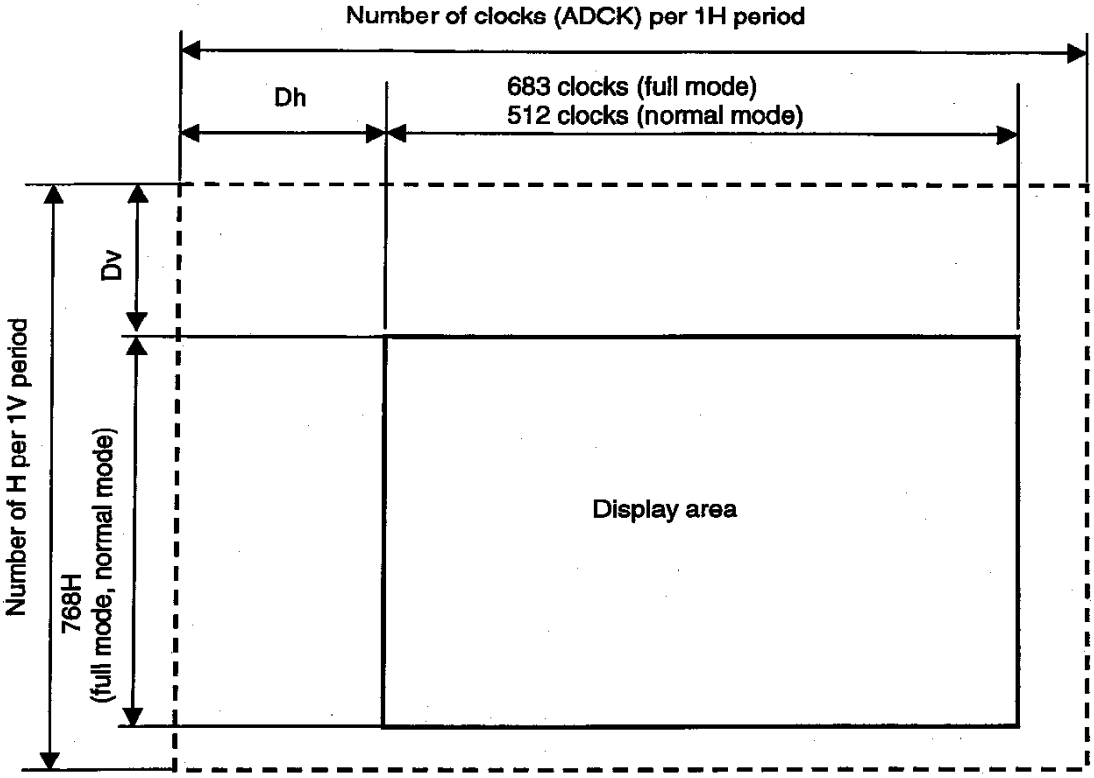


Type of serial interface connector

Module side connector:	FI-WE41P-HF
Mating connector:	FI-W41S (plug housing)
	FI-C3-A1-15000 (contact)
Connector supplier:	Japan Aviation Electronics Industry, Limited (JAE)
Fitting cable:	AWG#28 to 32 twist pair cable
	(Total cable assembly is recommend to be shielded)

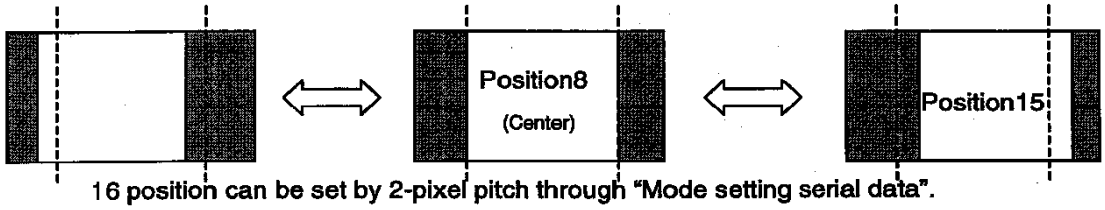
DISPLAY POSITION

The relation among Dv, Dh, and the display position is as shown below.



1) Setting range of Dv and Dh
   Dv: 9bit 0-511 line (HSYNC)
   Dh: 10bit 0-1023 dot (ADCK)
2) Limitation of number of clocks per 1H period
   normal mode: (Dh)+2+512 ≤ Number of clocks per 1H period ≤ 3071
   full mode: (Dh) +2+683 ≤ Number of clocks per 1H period ≤ 3071
3) Limitation of number of HSYNC pulses per 1V period
   (Dv) +2+768 ≤ Number of HSYNC pulses per 1V period ≤ 2047 (HSYNC)

Display position setting in normal modes (aspect ratio 4:3)

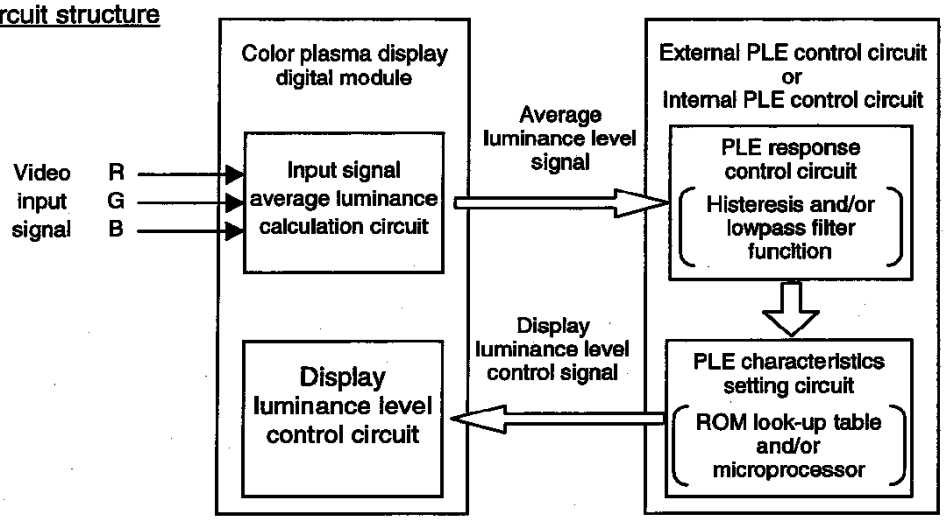


16 position can be set by 2-pixel pitch through "Mode setting serial data".

PLE (Peak Luminance Enhancement) FUNCTION

The PLE function makes it possible to increase the luminance level of the PDP display when the average luminance level of the input video signal is low. This PLE function reduces the maximum power by absorbing the luminance when the high-power-load-image is displayed, and results in a higher contrast level.

PLE circuit structure



This plasma display module has following two modes. These two modes can be selected by the mode control signal.

1. "Internal PLE" mode ---- Built-in PLE function in the PDP module itself. This PLE mode realizes one of the best PLE characteristics without any additional circuit. Therefore this mode is very convenient, and it is recommend to utilize this function actively.

2. "External PLE" mode --- Externally controlled PLE function from the customer's interface circuit. External PLE mode enable to make customer's original characteristics within the limitation range. The PLE characteristics is strongly related not only to the luminance characteristics of plasma display module but also to the power consumption and the generated heat, therefore it is required to obtain the acknowledgement of NEC concerning the external PLE characteristics to be set at the customer.

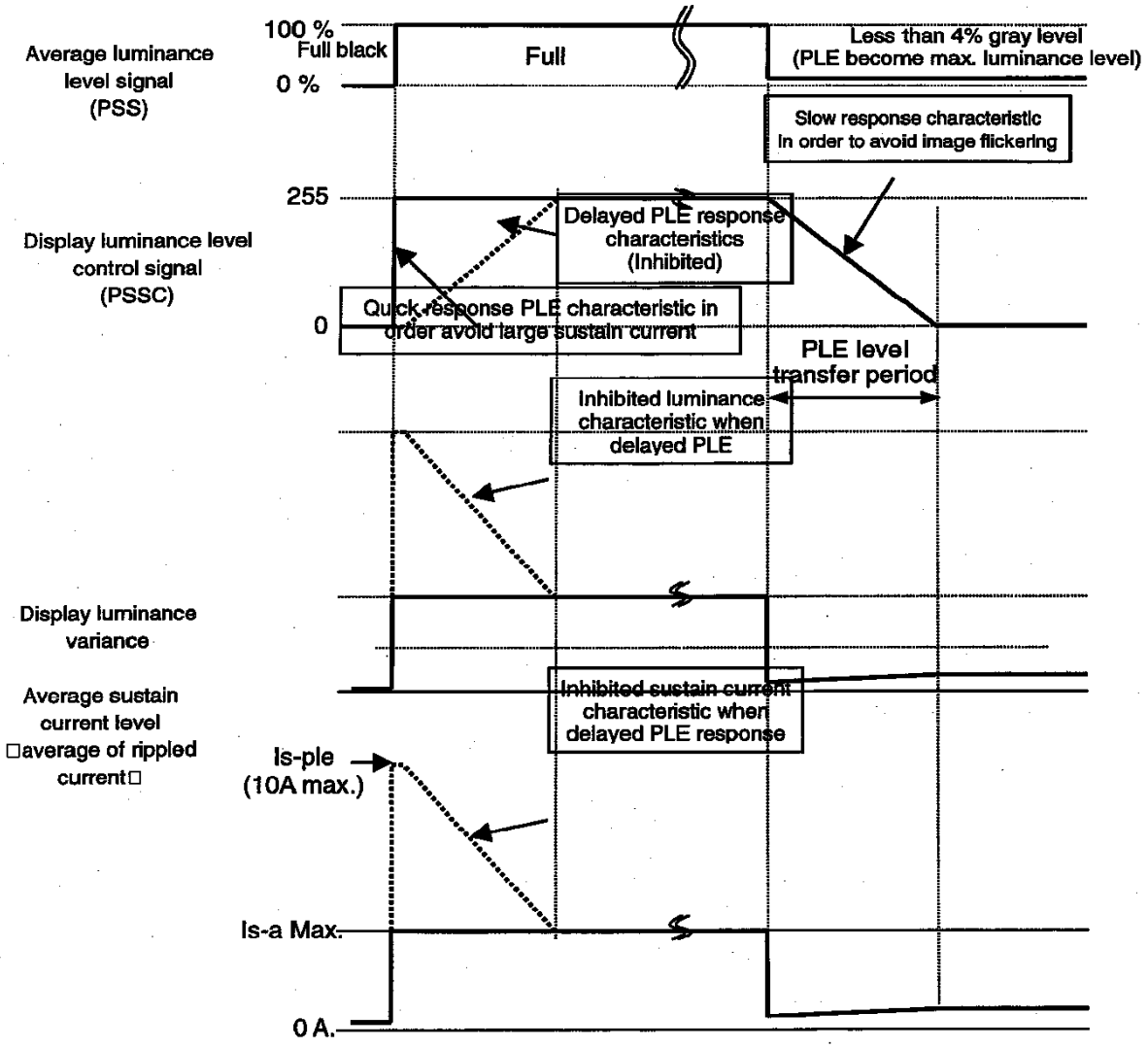
(Caution)
When use the external PLE function, please use within the limitation range. If external PLE characteristic is set outside of the limitation range, plasma display module may have a damage. Any trouble caused by this incorrect operation is not included in the warranty.

Power consumption and generated heat of plasma display module varies depending on the setting values of PLE characteristic. Therefore the temperature investigation and optimization of cooling design should be done in the state mounted in the plasma display set.

CHARACTERISTICS OF INTERNAL PLE

When PDP module displays full white with maximum luminance, or when PLE characteristic has some delayed response and display image is changed from full black to full white, large sustain current (Is-peak: 10A max.) flows, and plasma display becomes over power status.

In the internal PLE function, when the "Average luminance level" increases, in order to avoid large sustain current flow and over power status, the "Display luminance level" is immediately reduced to the setting level with quick response. And when display load decreases, in order to avoid image flickering caused by the short term average luminance level's fluctuations, the "Display luminance level" is gradually moved to the setting level with a slow response characteristic.
(Refer to the following figures)



CONNECTORS PIN ASSIGNMENT
(For the connector position, please refer to the Rear View in the Outline Drawing)

1. POWER INPUT CONNECTORS

Table 10. Connector CN104 Pin Assignment			
Pin No.	Symbol	Pin No.	Symbol
1	LVP	2	GND
3	GND	4	Vcc
5	GND	6	GND
7	Vd	8	N.C.
9	Vs	10	Vs

N.C.: non-connection pin.

Module side connector: B10PS-VH
Mating connector: VHR-10N (housing),
SVH-21T-P1.1(contact)
Connector supplier: J.S.T. TRADING COMPANY., LTD.
Fitting Cable: Equivalent to AWG#20

Table 11. Connector CN105 Pin Assignment			
Pin No.	Symbol	Pin No.	Symbol
1	Vs	2	Vs
3	N.C.	4	Vd
5	GND	6	GND
7	Vcc	8	GND
9	GND	---	---

N.C.: non-connection pin.

Module side connector: B9PS-VH
Mating connector: VHR-9N (housing),
SVH-21T-P1.1 (contact)
Connector supplier: J.S.T. TRADING COMPANY, LTD.
Fitting Cable: Equivalent to AWG#20

(Note): If using a long cable, applied voltage may be dropped because of its resistance.
Specified voltage should be applied correctly at the input of the module side connector.

2. SIGNAL INTERFACE CONNECTOR

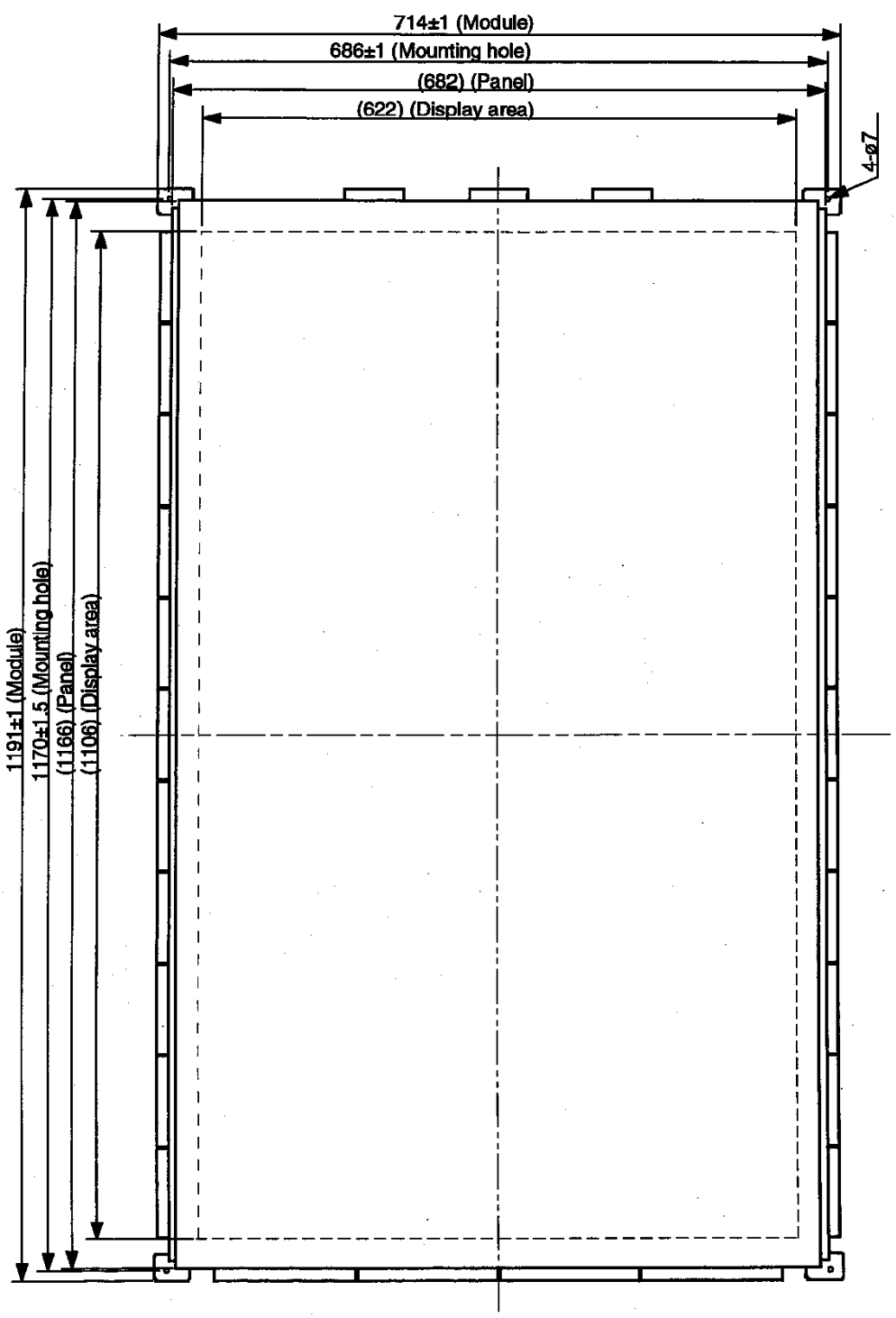
Table 12. Connector CN201 Pin Assignment

Pin No.	Symbol	Pin No.	Symbol
1	GND	2	LE
3	SCK	4	SDATA
5	ALARM	6	PSSC
7	CLE	8	PSS
9	PLE	10	PSCK
11	GND	12	RH+
13	RH-	14	GND
15	RCLK2+	16	RCLK2-
17	GND	18	RG+
19	RG-	20	GND
21	RF+	22	RF-
23	GND	24	RE+
25	RE-	26	GND
27	RD+	28	RD-
29	GND	30	RCLK+
31	RCLK-	32	GND
33	RC+	34	RC-
35	GND	36	RB+
37	RB-	38	GND
39	RA+	40	RA-
41	GND	---	---

Module side connector: FI-WE41P-HF
Mating connector: FI-W41S(housing),
FI-C3-A1-15000(contact)
Connector supplier: Japan Aviation Electronics Industry, Limited (JAE)
Fitting Cable: AWG#28 to 32 twist pair cable
(Total cable assembly is recommend to be shielded.)

(Note): If using a long cable, applied voltage may be dropped because of its resistance.
Specified voltage should be applied correctly at the input of the module side connector.

MECHANICAL DRAWING
FRONT VIEW (Unit: mm)



Note:The values in parentheses are for reference.

MECHANICAL DRAWING
REAR VIEW (Unit: mm)

T.B.D

IMAGE STICKING CHARACTERISTICS

1) Image sticking

The fluorescent substance used in the plasma module loses its luminance with the lapse of lighting time.
This deterioration in luminance appears to be a difference in luminance in relation to the surroundings, and comes to be recognized as image sticking.

In other words, the image sticking is defined as follows: when the same pattern (of the fixed display) is displayed for a long time, a difference in luminance is caused around the lighting area and non-lighting area due to deterioration in the fluorescent substance.
When the present pattern is changed over to another one, the boundary comes to be seen between the lighting area and non-lighting area due to difference in luminance in the pattern shown shortly before changeover. If this condition is accumulated, the boundary or image sticking comes to be seen with the naked eyes.

2) Secular change in luminance

The life of luminance, defined as the reduction to half of the initial level, is more than 10 thousand hours on average.
Conditions: All white (100% white) input at an ambient temperature of 25 °C.
However, this life time is not a guaranteed value for life and luminance. It should be recognized simply as the data for reference.

3) Warranty

Image sticking and faults in luminance and picture elements are excluded from the warranty objects.

4) Cause of deterioration in luminance

A major possible cause of deterioration in luminance is damage in the fluorescent substance due to impact caused by ions generated at the time of plasma discharges.

5) Practical value for image sticking

The relationship between integrated lighting time and luminance in this plasma module is described in the attached material. In particular, the deterioration in luminance tends to be accelerated up to 100 hours in the initial period. In the initial period, the fixed display of patterns particularly tends to cause image sticking.
The practical value for image sticking is difficult to define in concrete numerals. As described below, you are advised to take proper measures to make the occurrence of image sticking as slow as possible.

6) Proposed measures taken to relieve image sticking

So long as there is the reduction of luminance in the fluorescent substance, it is impossible to avoid the occurrence of image sticking. Therefore, to relieve image sticking, we offer you a method of entering an image input that may ensure reluctance to the generation of the difference in luminance reduction among the displayed dots.

The images from TV broadcasting involve a high rate of motion picture displays.
Therefore, there is less chance of being a cause of difference in luminance reduction among the cells. Even when the fixed patterns are displayed, they generally last for a few minutes.
Since the same pattern is less liable to be displayed, there is almost no influence toward image sticking.

If the fixed patterns tend to be displayed for a long time, however, there occurs a substantial imbalance between the lighting and non-lighting areas, thus causing a difference in luminance as a result. In this document, we offer you some proposals of installation, paying attentions to the two points: the reduction of difference in luminance achieved by integrated lighting time leveling and the method of edge smearing to make image sticking hard to be discerned.

The result from these proposals can, however, greatly depend on the contents of images and the operating environment. Therefore, we consider that it is essential to take the suitable measures in consideration of the customer's operating environment.

Example of Proposal 1:The display position is moved while the fixed display pattern is changed

over, or it is scrolled during the display.

Example of Proposal 2: If possible, a pattern of complementary color is incorporated (for integrated time leveling).

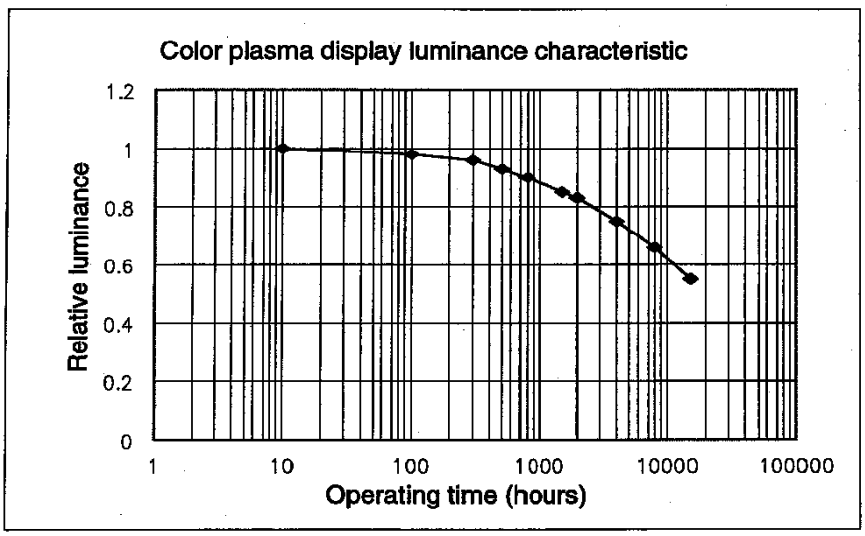
Example of Proposal 3: The fixed pattern and the motion picture display are reciprocally exchanged, in order to minimize the display period of the fixed pattern.

Example of Proposal 4: During operation, the luminance of screen is suppressed as low as possible. For the display patterns, characters are indicated not on the black ground (non-picture area) but on the colored ground (mixture of R, G, B recommended).

7) Proposed countermeasures for the plasma module

Since the PDP is a display that uses a fluorescent substance like the CRT, it is a fundamental phenomenon that image sticking occurs. Unlike the CRT, the PDP gives rise to deterioration in the fluorescent substance due to impact caused by ions generated during plasma display.

As a result of the above-mentioned improvements, it is possible to extend the PDP lifetime and relieve the effect of burning, but is impossible to realize the complete elimination of burning so far as a fixed pattern is displayed for a long time.



1. WARNING AND CAUTIONS

Warning: Indicates a hazard that can lead to death or injury if the warning is ignored and the product is handled incorrectly.
Caution: Indicates a hazard that can lead to injury or damage to property if the caution is ignored and the product is handled incorrectly

[Warning]

(1) This product uses a high voltage (420V max.). Do not touch the circuitry of this product with your hands when power is supplied to the product or immediately after turning off the power. Be sure to confirm that the voltage has dropped to a sufficiently low level.
(2) Do not supply a voltage higher than that specified to this product. This can damage the product and may cause a fire.
(3) Do not use this product in locations where the humidity is extremely high, where it may be splashed with water, or where it is surrounded by flammable materials. Do not install or use the product in a location that does not satisfy the specified environmental conditions. This can damage the product and may cause a fire.
(4) If a foreign substance (such as water, metal, or liquid) gets inside the product, immediately turn off the power. Continuing to use the product as it is may cause fire or electric shock.
(5) If the product emits smoke, an abnormal smell, or makes an abnormal sound, immediately turn off the power. If nothing is displayed or if the display goes out during use, immediately turn off the power. Continuing to use the product as it is may cause fire or electric shock.
(6) Do not disconnect or connect the connector while power to the product is on. It takes some time for the voltage to drop to a sufficiently low level after the power has been turned off. Confirm that the voltage has dropped to a safe level before disconnecting or connecting the connector. Otherwise, this may cause fire, electric shock, or malfunctioning.
(7) Do not pull out or insert the power cable from/to an outlet with wet hands. Doing so may cause electric shock.
(8) Do not damage or modify the power cable. Doing so it may cause fire or electric shock.
(9) If the power cable is damaged, or if the connector is loose, do not use the product; otherwise, this can lead to fire or electric shock.
(10) If the power connector or the connector of the power cable becomes dirty or dusty, wipe it with a dry cloth. Otherwise, this can lead to fire.

[Caution]

(1) Do not place this product in a location that is subject to heavy vibration, or on an unstable surface such as an inclined surface. The product may fall off or fall over, causing injuries.
(2) When moving the product, be sure to turn off the power and disconnect all the cables. While moving the product, watch your step. The product may be dropped or fall, leading to injuries or electric shock.
(3) Before disconnecting cables from the product, be sure to turn off the power. Be sure to hold the connector when disconnecting cables. Pulling a cable with excessive force may cause the core of the cable to be exposed or break the cable, and this can lead to fire or electric shock.
(4) This product should be moved by two or more persons. If one person attempts to carry this product alone, he/she may be injured.
(5) This product contains glass. The glass may break, causing injuries, if shock, vibration, heat, or distortion is applied to the product.
(6) The temperature of the glass surface of the display may rise to 50 C or more depending on the conditions of use. If you touch the glass inadvertently, you may be burned.
(7) Do not poke or strike the glass surface of the display with a hard object. The glass may break or be scratched. If the glass breaks, you may be injured.
(8) If the glass surface of the display breaks or is scratched, do not touch the broken pieces or the scratches with bare hands. You may be injured.
(9) Do not place an object on the glass surface of the display. The glass may break or be scratched.

2. Cautions on Design

(1) This product may be damaged if it is subject to excessive stresses (such as excessive voltage, current, or temperature). The absolute maximum ratings specify the limits of these stresses, and system design must ensure that none of the absolute maximum ratings are exceeded.
(2) The recommended operating conditions are conditions in which the normal operation of this product is guaranteed. All the rated values of the electrical specifications are guaranteed within these

conditions. Always use the product within the range of the recommended operating conditions. Otherwise, the reliability of the product may be degraded. Use of the product with a combination of parameters, conditions, or logic not specified in the specifications of this product is not guaranteed. If intending to use the product in such a way, be sure to consult NEC in advance.

(3) This product emits near infrared rays (800 to 1000 nm) that may cause the remote controllers of other electric products to malfunction. To avoid this, use an infrared absorption filter and thoroughly evaluate the system and environment.

(4) This product uses high-voltage switching and a high-speed clock. A system using this product should be designed so that it does not affect the other systems, and should be thoroughly evaluated.

(5) This product has a glass display surface. Design your system so that excessive shock and load are not applied to the glass. Exercise care that the vent at the corner of the glass panel is not damaged. If the glass panel or vent is damaged, the product is inoperable.

(6) There are some exposed components on the rear panel of this product. Touching these components may cause an electric shock.

(7) This product uses a high voltage. Design your system so that any residual voltage in this product is dissipated quickly when power is turned off, observing the specifications.

(8) This product uses heat-emitting components. Take the heat emitted by these components into consideration when designing your system. If the product is used outside the specified temperature range, it may malfunction.

(9) This product uses a high voltage and, because of its compact design, components are densely mounted on the circuit boards. If dust collects on these components, it can cause short-circuiting between the pins of the components and moisture can cause the insulation between the components to break down, causing the product to malfunction.

(10) Regulations and standards on safety and electromagnetic interference differ depending on the country. Design your system in compliance with the regulations and standards of the country for which your system is intended.

(11) To obtain approval under certain safety standards (such as UL and EN), a filter that passes a shock test must be fitted over the glass surface of the finished product. In addition, it must be confirmed that the level of UV emissions is within the range specified by such standards.

(12) If this product is used as a display board to display a static image, "image sticking" occurs. This means that the luminance of areas of the display that remain lit for a long time drops compared with the luminance of areas that are lit for a shorter time, causing uneven luminance across the display. The degree to which this occurs is in proportion to the luminance at which the display is used. To prevent this phenomenon, therefore, avoid static images as much as possible and design your system so that it is used at a low luminance, by setting PLE to the maximum level.

(13) Within the warranty period, general faults that occur due to defects in components such as ICs will be rectified by NEC without charge. **However, IMAGE STICKING is not included in the warranty.** Repairs due to the other faults may be charged for depending on responsibility for the faults.

(14) This product is designed to NEC's "Standard" quality grade. If you wish to use the product for applications outside the scope of the "Standard" grade, be sure to consult NEC in advance to assess the technological feasibility before starting to design your system.

3. Cautions on Use

(1) Because this product uses a high voltage, connecting or disconnecting the connectors while power is supplied to the product may cause malfunctioning. Never connect or disconnect the connectors while the power is on. Immediately after power has been turned off, a residual voltage remains in the product. Be sure to confirm that the voltage has dropped to a sufficiently low level.

(2) Watching the display for a long time can tire the eyes. Take a break at appropriate intervals.

(3) Do not cover or wrap the product with a cloth or other covering while power is supplied to the product.

(4) Before turning on power to the product, check the wiring of the product and confirm that the supply voltage is within the rated voltage range. If the wiring is wrong or if a voltage outside the rated range is applied, the product may malfunction or be damaged.

(5) Do not store this product in a location where temperature and humidity are high. This may cause the product to malfunction. Because this product uses a discharge phenomenon, it may take time to light (operation may be delayed) when the product is used after it has been stored for a long time. In this case, it is recommended to light all cells for about 2 hours (aging).

(6) If the glass surface of the display becomes dirty, wipe it with a soft cloth moistened with a neutral detergent. Do not use acidic or alkaline liquids, or organic solvents.

(7) This product is made from various materials such as glass, metal, and plastic. When discarding it, be sure to contact a professional waste disposal operator.

4. REPAIR AND MAINTENANCE

Because this product combines the display panel and driver circuits in a single module, it cannot be repaired or maintained at users' office or plant. Arrangements for maintenance and repair will be determined later.

5. OTHERS

(1) If your system requires the user to observe any particular precautions, in addition to the above warnings and cautions, include such caution and warning statements in the manual for your system.
(2) If you have any questions concerning design, such as on housing, storage, or operating environment, consult NEC in advance.

Revise history

Date	Contents	Remarks
May 9, 2000	Issue Preliminary(1) edition	